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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,190	04/04/2005	Tetsuro Sato	SAT026	9609

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EXAMINER	
YAARY, MICHAEL D	

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2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/530,190	SATO ET AL.	
	Examiner	Art Unit	
	MICHAEL YAARY	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/04/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-54 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 8-11, 14, 19, 20, 21, 23, 28-32, 45, 46, 49, and 52-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Perren (US Pat. 5,636,369).

4. **As to claims 1, 21, and 49,** Perren discloses a bit string check method including a process of checking against a plurality of bit patterns registered in advance at multiple stages with dividing a bit string to be searched into a plurality of partial-object bit strings (abstract), wherein a current stage being one check stage included in the multiple stages, comprising:

An all check step of selecting a partial-object bit string of the current stage from the bit string to be searched and comparing the partial-object bit string of the current stage with all possible values of a partial-object bit string of the current stage (column 1,

lines 52-54 discloses comparing a stream of n partial bits to a predetermined pattern of m bits);

A pattern loading step of loading a pattern table of the current stage from memory independently of the all check step before, after or in parallel with the all check step (look-up table, figure 5), the pattern table for indicating a partial registration bit pattern of each of the plurality of registration patterns, the pattern table having a range corresponding to all possible values of a partial-object bit string of the current stage, the pattern table being determined by check-continuation information received from a stage preceding the current stage (column 1, lines 54-67);

A judgment step of obtaining a check result indicating at least a presence or absence of the partial registration bit pattern of the current stage which matches the partial-object bit string of the current stage in accordance with the result of the all-check step and the pattern table of the current stage (column 1, lines 54-67);

an outputting step of outputting check-continuation information including the address of a pattern table of the stage subsequent to the current stage from an address table corresponding to the pattern table of the current stage in accordance with the check result (column 2, line 44-column 3, line 30).

5. **As to claims 3 and 23,** Perren discloses the outputting step outputs check-continuation information including the address of a pattern table of the next stage

subsequent to the matched partial registration bit patterns of the current stage (column 2, line 44-column 3, line 30).

6. **As to claims 8 and 28,** Perren discloses an updating step of adding or deleting a registration bit pattern by updating the pattern table and the address table (column 2, lines 54-58).

7. **As to claims 9 and 29,** Perren discloses the all-check step and the pattern loading step are executed in parallel (fig. 5).

8. **As to claim 11,** the claim is rejected for the same reasons as claims 8 and 9 above.

9. **As to claims 10 and 31,** Perren discloses a plurality of the check stages are executed in a pipeline (column 2, line 44-column 3, line 30).

10. **As to claims 14 and 32,** Perren discloses data including the check-continuation information is packetized and transmitted between the plurality of check stages (column 1, lines 14-22 and column 1, lines 54-67).

11. **As to claims 19 and 45,** Perren discloses checking the bit string to be searched by the method of claim 1; and managing data including the bit string to be searched on the basis of a checking result of the checking step (column 2, line 44-column 3, line 30).

12. **As to claims 20 and 46,** Perren discloses a step of checking by the checking method of claim 1 with regarding data forming an evaluation source of a state transition as the bit string to be searched, and with regarding data indicating a plurality of state transition conditions as the plurality of registration bit patterns; and a step of transiting states of a data processing circuit in accordance with a check result of the check step (column 1, lines 52-67).

13. **As to claim 30,** Perren discloses a classification device comprising a plurality of the check stages of claim 21 (device of figure 1 and 5).

14. **As to claims 52-54,** Perren discloses the all-check step, the check is preformed by hardware employing a comparator or a look-up table (look-up table figure 5).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 2, 22, 33-38, 42, 43, 47, 48, 50, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perren in view of Soo (US Pat. 5,570,306).

17. **As to claims 2 and 22,** Perren does not disclose the pattern table is mask data consisted of a bit flag indicating a validness or invalidness of the partial registration bit pattern. However, Soo discloses the pattern table is mask data consisted of a bit flag indicating a validness or invalidness of the partial registration bit pattern (column 2, lines 38-47 and column 5, lines 6-17, detecting masked occurrence patterns).

18. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Perren by the masked data, as taught by Soo, for the benefit of reducing processing time for recognizing bit patterns.

19. **As to claims 33 and 42,** the combination of Perren and Soo disclose a cache device for inputting and outputting data from and to the memory (Soo, column 4, lines 45-49).

20. **As to claims 34, 47, and 50,** the combination of Perren and Soo disclose the memory stores a check table including the pattern table and the address table, and the

size of a cache line of the cache device is equal to the size of the check table (Soo, column 7, lines 27-56).

21. **As to claims 35, 38, 43, 48, and 51,** the combination of Perren and Soo disclose receiving information of search types designating the first check table, and wherein the cache device comprises a management unit for allocating the cache line in a unit of each of types to be searched and the check device, and managing the cache line in a unit of each types to be searched and the check device (Soo, column 4, lines 45-49 and column 7, lines 27-56).

22. **As to claim 36,** the combination of Perren and Soo disclose means for receiving search type information designating a first check table, wherein the check table is stored in an individual address range allocated in a unit of each search type and each check stage, in the memory and wherein a cache line of the cache device is allocated in a unit of the individual address range (Soo, column 4, lines 45-49 and column 7, lines 27-56).

23. **As to claim 37,** the combination of Perren and Soo disclose when the check table is not an on-cache, the cache device informs this to the check device, stops the process of the check device and returns to a queue (Soo, column 4, lines 45-49 and column 7, lines 27-56).

24. Claims 4-7, 12, 13, 15-18, 25-27, 39-41, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perren in views of Sands (US Pat. 5,661,763).

25. **As to claims 4 and 24,** Perren does not disclose wherein the check result outputted from the judgment step further includes a presence or absence of a partial registration bit pattern having the maximum or minimum value closest to the partial-object bit string in the current stage, and wherein the check-continuation information of the outputting step further includes an address of a scope search pattern table of the next stage subsequent to the maximum or minimum partial registration bit pattern of the current stage (column 2, lines 48-64).

26. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Perren by applying maximum pattern match of the bit string, as taught by Sands, for the benefit of applying a user programmable bit pattern where both the contents and the bit length are programmable.

27. **As to claims 5 and 25,** the combination of Perren and Sands disclose a candidate address storing step of storing the address of the scope search pattern table when the matched partial registration bit pattern of the current stage is present and when the maximum or minimum partial registration bit pattern of the current stage is present, wherein the check-continuation information of the outputting step further

includes the candidate address when the matched partial registration bit patter of the current stage is not present and when the maximum or minimum partial registration bit pattern of the current stage is not present (Sands, column 2, line 48-column 3, line 17).

28. **As to claims 6 and 26,** the combination of Perren and Sands disclose bypassing the all check step and the judgment step when the check-continuation information including the address of the scope search pattern table is given, wherein the check-continuation information of the outputting step further includes the address of the pattern table of the next stage subsequent to the maximum or minimum partial registration bit pattern shown on the pattern table, from the address table corresponding to the scope search pattern table (Sands, column 7, lines 10-37).

29. **As to claims 7, 12, and 27,** the combination of Perren and Sands disclose the pattern table further includes bypass data indicating the maximum or minimum registration bit pattern determined in correspondence with the maximum or minimum partial registration bit pattern shown on the pattern table, wherein the check method further comprises the step of bypassing the all-check step, the pattern loading step, and the judgment step when the check-continuation information including the address of the scope search pattern table is given, and wherein the outputting step outputs the final check information including the bypass data corresponding to the scope search pattern table to terminate the check of the bit string to be searched (Sands, column 2, line 48-column 3, line 17 and column 7, lines 10-37).

30. **As to claim 13,** the claim is rejected for similar reasons as claims 4 and 5 above.

31. **As to claims 15 and 39,** the combination of Perren and Sands disclose a classification process including the plurality of check stages of claim 4, wherein the registration bit pattern indicates a scope including a plurality of classification results (Perren, column 2, lines 44-67).

32. **As to claims 16 and 40,** the combination of Perren and Sands disclose the plurality of classification processes; and a logical operation process for performing a logical AND of the plurality of classification results included in a plurality of scopes obtained through the plurality of classification processes to obtain a final classification result (Sands, column 4, line 42-column 5, line 15).

33. **As to claims 17 and 41,** the combination of Perren and Sands disclose the logical operation process performs a matrix operation of the logical AND of the plurality of classification results to obtain the final classification result (Sands, column 4, line 42-column 5, line 15).

34. **As to claims 18 and 44,** the combination of Perren and Sands disclose checking the scope to which the bit string to be searched belongs by the classification method of claim 15, with regarding a bit string to manage a packet including at least on of an IP

address, a port number, and a protocol as the bit string to be searched; and managing the packet including the bit string to be searched on the basis of classification result of the scope to which the bit string to be searched belongs (Perren, column 1, lines 45-67).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Pat. 4,734,676 – Method and device for detecting a particular bit

US Pat. 5,526,298 – Random unique word detection

US Pat. 5,764,708 – Identifying predetermined sequence

US Pat. 5,894,427 – Concurrent detection of bit patterns

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL YAARY whose telephone number is (571)270-1249. The examiner can normally be reached on Mon-Fri 9 a.m.-5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on 571-272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. Y./
Examiner, Art Unit 2193

/Lewis A. Bullock, Jr./
Supervisory Patent Examiner, Art Unit 2193